L Number	Hits	Search Text	DB	Time stamp
1	3	(716/$).ccls. and (logic adj circuit) and (add$ adj information) and (passive adj component)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/20 10:59
2	0	(logic adj circuit) and (addition adj information) and (passive adj component)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/20 11:00
3	1	(logic$ adj circuit) and (addition adj information) and (passive adj component)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/20 11:02
4	1	(logic$ adj circuit) and (deletion adj information) and (passive adj component)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/20 11:04
-	28	(716/$).ccls. and ((logical adj circuit) same (file or stor$))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/06 16:55
-	0	(wiring adj modification) and ((logical adj circuit) same (file or stor$))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/06 18:02
-	0	(716/$).ccls. and (topology adj table) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 13:41
-	12	(716/$).ccls. and (topology) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 14:32
-	129	(topology) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 14:38
-	1	(topology) and (passive adj component) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 14:45
-	13	(passive adj component) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 14:55
-	0	((delay adj line) adj (data or information)) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 15:08
-	219	(delay adj line) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 15:52

-	4	(part adj list) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 15:57
-	0	(logical adj circuit) and ((passive adj component) adj (delection adj information))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 17:11
-	9	(logical adj circuit) and (resistance and capacitance) and (peradj unit adj length)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 17:13
-	12	(logical adj circuit) and (resistance and capacitance) and (per adj unit adj length)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 17:42
-	1307	(table same (resistance and capacitance))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 17:44
-	68	(716/$).ccls. and (table same (resistance and capacitance))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 17:46
-	57	(716/$).ccls. and (rout$ or wir$) and (table same (resistance and capacitance))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 18:06
-	7	(wire same (edit or modify)) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 15:14
-	0	((wire adj editing) adj unit) and (logic$ adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 15:46
-	1	(wire adj editing) and (logic$ adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 15:51
-	10	((logic$ adj circuit) adj modification)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 16:49
-	0	(wire adj editing) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 16:51
-	0	(line adj editing) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 16:53

-	8	(rerouting) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 17:55
-	0	(wire adj modification) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 17:56

L Number	Hits	Search Text	DB	Time stamp
1	89	(logical adj circuit) and (inductor)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/20 13:34
-	28	(716/$).ccls. and ((logical adj circuit) same (file or stor$))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/06 16:55
-	0	(wiring adj modification) and ((logical adj circuit) same (file or stor$))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/06 18:02
-	0	(716/$).ccls. and (topology adj table) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 13:41
-	12	(716/$).ccls. and (topology) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 14:32
-	129	(topology) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 14:38
-	1	(topology) and (passive adj component) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 14:45
-	13	(passive adj component) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 14:55
-	0	((delay adj line) adj (data or information)) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 15:08
-	219	(delay adj line) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 15:52
-	4	(part adj list) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 15:57
-	0	(logical adj circuit) and ((passive adj component) adj (delection adj information))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 17:11
-	9	(logical adj circuit) and (resistance and capacitance) and (peradj unit adj length)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 17:13

-	12	(logical adj circuit) and (resistance and capacitance) and (per adj unit adj length)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 17:42
-	1307	(table same (resistance and capacitance))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 17:44
-	68	(716/$).ccls. and (table same (resistance and capacitance))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 17:46
-	57	(716/$).ccls. and (rout$ or wir$) and (table same (resistance and capacitance))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/07 18:06
-	7	(wire same (edit or modify)) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 15:14
-	0	((wire adj editing) adj unit) and (logic$ adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 15:46
-	1	(wire adj editing) and (logic$ adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 15:51
-	10	((logic$ adj circuit) adj modification)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 16:49
-	0	(wire adj editing) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 16:51
-	0	(line adj editing) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 16:53
-	8	(rerouting) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 17:55
-	0	(wire adj modification) and (logical adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/14 17:56
-	3	(716/$).ccls. and (logic adj circuit) and (add$ adj information) and (passive adj component)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/20 10:59

-	0	(logic adj circuit) and (addition adj information) and (passive adj component)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/20 11:00
-	1	(logic$ adj circuit) and (addition adj information) and (passive adj component)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/20 11:02
-	1	(logic$ adj circuit) and (deletion adj information) and (passive adj component)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/20 11:04
-	1	(logical adj circuit) and (part adj list)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/20 12:46
-	10	(logical adj circuit) and (component adj (list or table))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/20 13:30